Mercury Analog Output DAC Circuit Description
Revision: 1
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1. Applicability

This document applies to Mercury Main Board schematic 03-925060-00, Revision PR4.

2. Circuit description

There are three analog output DACs on the Main Board, each consisting of a pulse-width modulator and a low-pass filter. A single 16-bit counter, clocked at 25MHz, serves all three DACs. Each DAC has its own 16-bit latch and a digital comparator, which compares the value in the latch with the counter value. Every 2.5ms, the counter is reset, and the latches are reloaded with values calculated in software. The pwm output flip-flops are set at this time also. When the counter reaches the value stored in one of the latches, the associated comparator clears the output flip-flop for that DAC. All of this digital circuitry is contained in FPGA X4.

The pwm output signals from X4, along with their complements, control analog switches U3 and U12. The switch sections are connected in pairs, alternately switching the common point of each pair between +10V and -1V as the associated pwm signal changes state. AR4 (pins 1-3), along with two sections of R4, generates the -1V reference for all three DACs. Although the resistors have absolute accuracies of only ±1%, their temperature coefficients track to ±10ppm/°C, so drift is minimal after initial calibration. R44 and C53 minimize the glitches at the output of AR4 when U3 and U12 switch, thus reducing nonlinearities and crosstalk between the DACs.

Each pwm output from a switch pair is applied to a low pass filter, composed of two identical sections in cascade. These active filters utilize the popular Sallen-Key configuration, which has unity gain (non-inverting) at DC. The 100pF capacitors between the amplifier inputs have been added to eliminate interference from digital sources. The filters have four repeated real poles at 15.4Hz. While the roll-off of this design is rather slow above the cutoff frequency, the step response has no overshoot, which is desirable for chromatographic signals. The resistive voltage dividers at the amplifier outputs (e.g., R45 and R46) reduce the output signal range by a factor of 10, to span +1V to -0.1V.

With a clock frequency of 25MHz, the DAC counter can accumulate only 62,500 counts during its 2.5ms counting period. This would appear to limit the maximum resolution of the DACs to 16 bits, well below the required value of 20 bits. However, the low pass filters can average many successive output values from the counters, so the resolution can be enhanced by dithering the DAC count between two adjacent values. One microvolt resoultion is achieved at the DAC outputs by this technique. Waveforms observed at the

pwm inputs to switches U3 and U12 will normally have an apparent "jitter" in pulse width of 40ns as the software switches the count value up and down.

Variations in component values can cause small changes in the scale and offset factors for the DACs. The DAC outputs are fed to the ADC input multiplexer, so software can correct the digital output values to result in accurate analog voltages.

3. Log of revisions and file identification

Rev. 1 9/29/95

File: ENGRSERV:\3800ELEC\MB\DAC\DACCD.DOC

Author: D. DeFord